PRECISION CLOSED LOOP DELAY LINE FOR WIDE FREQUENCY DATA RECOVERY

Abstract of the Disclosure

A closed loop delay line system (700) includes a phase lock loop that provides a phase lock output signal (715). A delay line (702) includes a clock input, a delay line output, and a delay line bias input. A bias signal provided to the delay line bias input (727) adjusts the speed of the delay line (702). A phase detector (720) compares phase between a first timing signal input (704) and the delay line output (706). A bias adjust circuit (726) mixes the phase compare output signal (725) and the phase lock output signal (715) to provide a combination bias signal (727) to the delay line (702). Additionally, the relative timing position of strobe outputs (734) from the delay line (702) can be individually adjusted.